UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/727,102	12/02/2003	Jens Barrenscheen	J0658.0018	4397

38881 7590 07/16/2009

DICKSTEIN SHAPIRO LLP
1177 AVENUE OF THE AMERICAS 6TH AVENUE
NEW YORK, NY 10036-2714

EXAMINER	
LEE, CHUN KUAN	

ART UNIT	PAPER NUMBER
2181	

MAIL DATE	DELIVERY MODE
07/16/2009	PAPER

Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

UNITED STATES PATENT AND TRADEMARK OFFICE

Commissioner for Patents
United States Patent and Trademark Office
P.O. Box 1450
Alexandria, VA 22313-1450
www.uspto.gov

BEFORE THE BOARD OF PATENT APPEALS AND INTERFERENCES

Application Number: 10/727,102
Filing Date: December 02, 2003
Appellant(s): BARRENSCHEEN ET AL.

Laura C. Brutman
For Appellant

EXAMINER'S ANSWER

This is in response to the appeal brief filed 04/29/2009 appealing from the Office action mailed 04/15/2008.

(1) Real Party in Interest

A statement identifying by name the real party in interest is contained in the brief.

(2) Related Appeals and Interferences

The examiner is not aware of any related appeals, interferences, or judicial proceedings which will directly affect or be directly affected by or have a bearing on the Board's decision in the pending appeal.

(3) Status of Claims

The statement of the status of claims contained in the brief is correct.

(4) Status of Amendments After Final

No amendment after final has been filed.

(5) Summary of Claimed Subject Matter

The summary of claimed subject matter contained in the brief is correct.

(6) Grounds of Rejection to be Reviewed on Appeal

The appellant's statement of the grounds of rejection to be reviewed on appeal is correct.

(7) Claims Appendix

The copy of the appealed claims contained in the Appendix to the brief is correct.

(8) Evidence Relied Upon

Applicant's Admitted Prior Art (AAPA)	Specification, [0002]-[0029] and Drawings, Figure 1	
US Publication 2003/0103519	Balasundram et al.	06-2003
US Patent 3,985,962	Jones et al.	10-1976
US Patent 6,772,251	Hastings et al.	08-2004

US Patent 6,154,509	Bishop	11-2000
US Patent 6,578,940	Rehmann et al.	06-2003
"Data Communications Basics"		10-1997

(9) Grounds of Rejection

The following ground(s) of rejection are applicable to the appealed claims:

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

1. Claims 2-4, 6-8, 10, 12 and 23-25 are rejected under 35 U.S.C. 103(a) as being unpatentable over Applicant's Admitted Prior Art (AAPA) in view of Balasundram et al. (US Pub.: 2003/0103519).

2. As per claims 23-24, AAPA teaches an arrangement comprising:

a first semiconductor chip (Drawings, MC of Fig. 1 and Specification, [0002]-[0003]); and

a second semiconductor chip (Drawings, PC of Fig. 1 and Specification, [0002]-[0003]) which is connected to and drives electrical loads based on a timing defined by load control data (Specification, [0002] and [0004]-[0005]);

a first data communication means for the second semiconductor chip transmitting diagnostic data, which represent at least one of states prevailing in and events occurring in the second semiconductor chip, to the first semiconductor chip (Specification, [0002] and [0011]);

a load control data line (Drawings, DATA2 of Fig. 1) utilized by the first semiconductor chip transmitting the load control data which control the second semiconductor chip (Specification, [0002] and [0008]-[0009]);

a pilot data line (Drawings, DATA1a of Fig. 1) utilized by the first semiconductor chip transmitting the pilot data which control the second semiconductor chip (Specification, [0002] and [0008]-[0009]); and

a chip select line associated with each of the load control data line (CS2 of Fig. 1) and a pilot data line (CS1 of Fig 1), wherein the chip select line include data designating the start and the end of the transmission of the corresponding data intended for the second semiconductor chip (e.g. PC) (Specification, [0022]-[0026]).

AAPA does not teach the arrangement comprising:

the plurality of second semiconductor chips;

a single, second data communication means for the first semiconductor chip … ; and

wherein the load control data and the pilot data are transmitted …; and

wherein a first portion of data transmitted in a frame … .

Balasundram teaches a system and a method comprising:

transferring two or more messages (e.g. data) on the same communication line, by utilizing multiplexing technique such as time division multiplexing (TDM) ([0006] and [0008]-[0009]);

wherein the transferring of data is sent from a single central transmitter to the plurality of receivers ([0007] and [0046]), as data is transferred between a remote vehicle system controller (e.g. single transmitter) and a plurality of vehicle functions (e.g. plurality of receivers); and

wherein the plurality of data are transferred via an allotted particular time interval (e.g. units of frames) ([0008] and [0046]), wherein it would have been obvious for the plurality of data to be transferred utilizing a single allotted time interval (e.g. single frame), therefore the single allotted time interval is utilized for transferring the plurality of data.

It would have been obvious to one of ordinary skill in this art, at the time of invention was made to include Balasundram's transferring of data utilizing TDM into AAPA's arrangement for the benefit of reducing the overall number of wires utilized (Balasundram, [0006]) to obtain the invention as specified in claims 23-24. The resulting combination of the references further teaches the arrangement comprising:

the single transmitter (e.g. first semiconductor chip) is transferring data to the plurality of receivers (e.g. plurality of second semiconductor chips);

transferring two or more data (e.g. load control data and pilot control data) on the same communication line utilizing time division multiplexing in the allotted particular time interval (e.g. units of frames);

the chip select line associated with each of the second semiconductor chip (e.g. first, second semiconductor chip associated with load control data and second, second semiconductor chip associated with the pilot control data); and

by transferring the plurality of data utilizing the single allotted time interval (e.g. frame), it would have been obvious that in the single allotted time interval, the first portion of the allotted time interval have the first data directed towards a first receiver (e.g. first, second semiconductor chip) and the second portion of the time interval have the second data directed towards a second receiver (e.g. second, second semiconductor chip) as designated by data on the chip select line.

3. As per claim 25, AAPA teaches a method for communicating in an arrangement having a first semiconductor chip (Drawings, MC of Fig. 1) and a second semiconductor chip (Drawings, PC of Fig. 1) which is connected to and drives electrical loads based on a timing defined by load control data (Specification, [0002]-[0003]), comprising:

the second semiconductor chip transmitting diagnostic data, which represent at least one of states prevailing in and events occurring in the second semiconductor chip, via a first data line (Drawings, DATA1b of Fig. 1) to the first semiconductor chip (Specification, [0002] and [0011]);

the first semiconductor chip transmitting the load control data, which control the second semiconductor chip, via a load control data line (Drawings, DATA2 of Fig. 1) (Specification, [0002] and [0008]-[0009]);

the first semiconductor chip transmitting the pilot data, which control the second semiconductor chip, via a pilot data line (Drawings, DATA1a of Fig. 1) (Specification, [0002] and [0008]-[0009]); and

transmitting a chip select signal on a chip select line (CS1 and CS2 of Fig. 1), wherein the chip select line include data designating the start and the end of the transmission of the corresponding data intended for the second semiconductor chip (e.g. PC) (Specification, [0022]-[0026]).

AAPA does not teach the method comprising:

the plurality of second semiconductor chips;

the transmission of the load control data and pilot data …;

wherein the load control data and the pilot data are transmitted in units of frames …; and

wherein a first portion of data transmitted in a frame … .

Balasundram teaches a system and a method comprising:

transferring two or more messages (e.g. data) on the same communication line, by utilizing multiplexing technique such as time division multiplexing (TDM) ([0006] and [0008]-[0009]);

wherein the transferring of data is send from a single central transmitter to the plurality of receivers ([0007] and [0046]), as data is transferred between a remote vehicle system controller (e.g. single transmitter) and a plurality of vehicle functions (e.g. plurality of receivers); and

wherein the plurality of data are transferred via an allotted particular time interval (e.g. units of frames) ([0008] and [0046]), wherein it would have been obvious for the plurality of data to be transferred utilizing a single allotted time interval (e.g. single frame), therefore the single allotted time interval is utilized for transferring the plurality of data.

It would have been obvious to one of ordinary skill in this art, at the time of invention was made to include Balasundram's transferring of data utilizing TDM into AAPA's arrangement for the benefit of reducing the overall number of wires utilized (Balasundram, [0006]) to obtain the invention as specified in claim 25. The resulting combination of the references further teaches the arrangement comprising:

the single transmitter (e.g. first semiconductor chip) is transferring data to the plurality of receivers (e.g. plurality of second semiconductor chips);

transferring two or more data (e.g. load control data and pilot control data) on the same communication line utilizing time division multiplexing in the allotted particular time interval (e.g. units of frames); and

by transferring the plurality of data utilizing the single allotted time interval (e.g. frame), it would have been obvious that in the single allotted time interval, the first portion of the allotted time interval have the first data directed towards a first receiver (e.g. first, second semiconductor chip) and the second portion of the time interval have the second data directed towards a second receiver (e.g. second, second semiconductor chip) as designated by data on the chip select line.

4. As per claim 2, AAPA and Balasundram teach all the limitations of claim 23 as discussed above, where AAPA further teaches the arrangement comprising wherein the first semiconductor chip is a program-controlled unit (AAPA, Drawings, MC of Fig. 1).

5. As per claim 3, AAPA and Balasundram teach all the limitations of claim 23 as discussed above, where AAPA further teaches the arrangement comprising wherein the second semiconductor chip is a power chip (AAPA, Drawings, PC of Fig. 1).

6. As per claim 4, AAPA and Balasundram teach all the limitations of claim 23 as discussed above, where AAPA further teaches the arrangement comprising wherein the second data line is part of a second transmission channel which comprises:

a transmission clock line (AAPA, Drawings, CLK1, CLK2 of Fig. 1) via which the first semiconductor chip transmits a transmission clock signal to the second semiconductor chip (AAPA, Specification, [0021]-[0022] and [0024]-[0025]);

the second data line via which the first semiconductor chip transmits the load control data and the pilot data to the second semiconductor chip in time with the transmission clock signal (AAPA, Specification, [0021]-[0022] and [0024]-[0025]); and

a chip select line (AAPA, Drawings, CS1, CS2 of Fig. 1) via which the first semiconductor chip transmits the chip select signal to the second semiconductor chip, the chip select signal signaling to the second semiconductor chip the start and end of the transmission of data intended for the second semiconductor chip via the second data line (AAPA, Specification, [0021]-[0022] and [0024]-[0025]).

7. As per claim 6, AAPA and Balasundram teach all the limitations of claim 23 as discussed above, where AAPA further teaches the arrangement comprising wherein the first semiconductor chip defines time windows (e.g. a particular time interval) of constant length and transmits in each time window either the load control data frame or the pilot data frame or no data (AAPA, Specification, [0002]-[0005] and [0008]-[0009]), as the microcontroller (i.e. first semiconductor chip) controls and configures the power chip (i.e. second semiconductor chip) and that the power chip does nothing other than drive the electrical loads base on the stipulation received from the microcontroller, it would then be obvious for the microcontroller to define the time windows for transferring the corresponding data.

8. As per claim 7, AAPA and Balasundram teach all the limitations of claim 6 as discussed above, where both further teach the arrangement comprising wherein the first semiconductor chip transmits no further load control data frame for a respective length of n time windows after transmission of a load control data frame, where $n \geq 0$ and where n can be set by the user of the arrangement (AAPA , Specification, [0008]-[0009] and Balasundram, [0014], [0039]), as the multiplexing operates in a cyclical manner and the transferred message may have up to six instructive frames (Balasundram, Fig. 1, ref. 24-34), wherein the message is operate repetitively; therefore, the transferring of data may comprise the load control data frame following by the pilot data frame for configuring the second semiconductor into the sleep mode, thus the transferring of the

load control data frame may have been stopped for the period of n ≥ 0 frame, as the second semiconductor is in the sleep mode.

9. As per claim 8, AAPA and Balasundram teach all the limitations of claim 7 as discussed above, where Balasundram further teaches the arrangement comprising wherein a pilot data frame can be transmitted only in a time window in which no load control data frame is to be transmitted (Balasundram, Fig. 1 and [0008]), as each frame is allocated for a particular time interval, wherein each interval is for transferring a single message; therefore while the load control data frame is being transferred, the pilot data frame can not be transferred and vice versa.

10. As per claim 10, AAPA and Balasundram teach all the limitations of claim 23 as discussed above, where Balasundram further teaches the arrangement comprising wherein the first data line is part of a first transmission channel, and the first data line is used to transmit neither load control data nor pilot data (Balasundram, [0006]-[0009]), as the load control data and the pilot data are to be multiplexed over the single second communication line, therefore the transferring of these data would not utilize the first data line.

11. As per claim 12, AAPA and Balasundram teach all the limitations of claim 23 as discussed above, where AAPA further teaches the arrangement comprising wherein the first semiconductor chip transmits appropriate pilot data in order to prescribe to the

second semiconductor chip what transmission rate is to be used by the second semiconductor chip to transmit the diagnostic data to the first semiconductor chip (AAPA, Specification, [0009]), as the pilot data is utilized for setting the second semiconductor chip in modes including normal mode and sleep mode, therefore the corresponding mode, set by the pilot data would prescribe the transmission rate of the diagnostic data, such as having the normal rate during the normal mode or having the lower rate during the sleep mode.

12. Claim 9 is rejected under 35 U.S.C. 103(a) as being unpatentable over AAPA in view of Balasundram et al. (US Pub.: 2003/0103519) as applied to claim 6 above, and further in view of Jones et al. (US Patent 3,985,962).

AAPA and Balasundram teach all the limitations of claim 6 as discussed above, but AAPA and Balasundram do not expressly teach the arrangement comprising wherein transmission of the pilot data has priority when load control data and pilot data are awaiting transmission simultaneously.

Jones teaches a system and a method comprising a priority scheme such that when service request occurs simultaneous, the one with the higher priority is serviced prior to the others having lower priority (col. 1, ll. 15-37).

It would have been obvious to one of ordinary skill in this art, at the time of invention was made to include Jones's priority scheduling into AAPA and Balasundram's apparatus for the benefit of enabling the proper processing of simultaneous request in the system utilizing time-division multiplexing communication

(Jones, col. 1, ll. 15-37) to obtain the invention as specified in claim 9. The resulting combination of the references further teaches the apparatus comprising when transferring of load control data and pilot data occurs simultaneous, pilot data would have higher priority to be transferred before transferring the load control data, because the pilot data is utilized for configuring the operation of the second semiconductor chip; such that, when the second semiconductor chip is in sleep mode and the attempt to transfer load control data and pilot data occurs simultaneous, the pilot data would need to be transferred first to configure the second semiconductor to normal mode (e.g. awake mode) before sending the load control data for processing and execution.

13. Claims 11, 15 and 17 are rejected under 35 U.S.C. 103(a) as being unpatentable over AAPA in view of Balasundram et al. (US Pub.: 2003/0103519) as applied to claim 23 above, and further in view of "Data Communications Basics".

14. As per claims 11 and 17, AAPA and Balasundram teach all the limitations of claim 23 as discussed above, where AAPA further teaches the arrangement comprising wherein the transmission of data (AAPA, Drawings, DATA1a, DATA2 of Fig. 1) is accompany by the corresponding clock signal (AAPA, Drawings, CLK1, CLK2 of Fig. 1), as the first semiconductor chip (e.g. master) transmits the transmission clock signal to the second semiconductor chip (e.g. slave) (AAPA, Specification, [0021]-[0022] and [0024]-[0025]).

AAPA and Balasundram do not expressly teach the arrangement wherein the diagnostic data are transmitted in synch with a transmission clock signal generated in the second semiconductor chip and wherein this transmission clock signal is not transmitted to the first semiconductor chip; and wherein the second semiconductor chip transmits the diagnostic data in synch with the transmission clock signal received from the first semiconductor chip.

"Data Communications Basics" teaches a communication system and method comprising the receiver (i.e. second semiconductor chip) receiving the transmitter's internal clock (i.e. first semiconductor chip's transmission clock signal) and the transmitter's data, the receiver then synchronizes the receiver's local oscillator to the transmitter's local oscillator, wherein said receiver's local oscillator generates the respective receiver's internal clock (i.e. second semiconductor chip's transmission clock) and the data generated by the receiver to be transmitted to the transmitter utilizes the receiver's internal clock, therefore said data generated by the receiver would be in synch with the transmitter's internal clock, wherein the receiver does not transmit the receiver's internal clock to the transmitter (i.e. first semiconductor chip) (Asynchronous vs. Synchronous Transmission Section on page 4).

It would have been obvious to one of ordinary skill in this art, at the time of invention was made to include Data Communications Basics' communication system and method into AAPA and Balasundram's arrangement for the benefit of providing a more robust asynchronous data transferring and receiving system and method to obtain the invention as specified in claims 11 and 17.

15. As per claim 15, AAPA, Balasundram and "Data Communications Basics" teach all the limitations of claim 11 as discussed above, where Balasundram further teaches the arrangement comprising wherein the diagnostic data are transmitted in units of frames (e.g. particular time interval) (Balasundram, [0008]), where a frame starts with a start bit (e.g. leading component of "1") (Balasundram, Fig. 3, ref. 52) having a prescribed value and ends with one or two stop bits (Balasundram, Fig. 3, ref. 58) having prescribed values (e.g. having value of "0") (Balasundram, [0039] and [0042]-[0043]).

16. Claims 13-14 and 22 are rejected under 35 U.S.C. 103(a) as being unpatentable over AAPA in view of Balasundram et al. (US Pub.: 2003/0103519) as applied to claims 12 and 23 above, and further in view of Hastings et al. (US Patent 6,772,251).

17. As per claim 13, AAPA and Balasundram teach all the limitations of claim 12 as discussed above.

AAPA and Balasundram do not expressly teach the arrangement comprising wherein the transmission rate is prescribed by transmitting a division factor, and wherein the second semiconductor chip (e.g. slave) divides the frequency of a transmission clock signal transmitted to it by the first semiconductor chip (e.g. master) by the division factor and transmits the diagnostic data to the first semiconductor chip in time with the resultant signal.

Hastings teaches a system and a method for transferring serial data between a master (Fig. 1, ref. 110) and a slave (Fig. 1, ref. 120), comprising of a clock divider (Fig. 1, ref. 122) at the slave for dividing down the clock frequency from the master, and transfer data from the slave to the master using this resulting clock frequency (Fig. 1, col. 1, ll. 29-36; col. 2, ll. 60-67 and col. 3,ll. 1-21).

It would have been obvious to one of ordinary skill in this art, at the time of invention was made to include Hastings's division of the clock into AAPA and Balasundram's arrangement for the benefit of reducing the number of wires needed and increase data flow by reducing the flow of start and stop bits (Hastings, col. 1, ll. 29-55) to obtain the invention as specified in claim 13.

18. As per claim 14, AAPA, Balasundram and Hastings teach all the limitations of claim 13 as discussed above, where AAPA further teaches teach the arrangement comprising the transmission clock signal supplied to the second semiconductor chip (e.g. slave) represent the transmission clock, which is used by the first semiconductor chip (e.g. master) to transmit the load control data or pilot data signal to the second semiconductor chip (e.g. slave) (AAPA, Drawings, CLK1, CLK2, Data1a, Data2 of Fig. 1 and Specification, [0021]-[0025]).

19. As per claim 22, AAPA and Balasundram teach all the limitations of claim 23 as discussed above, where both further teach the arrangement comprising wherein the first semiconductor chip (e.g. single center transmitter) is connected to a plurality of second

semiconductor chips (e.g. receivers) (Balasundram, [0007]), every second semiconductor chip is connected to the first semiconductor chip via a dedicated chip select line (AAPA, Drawings, CS1, CS2 of Fig. 1), and chip select signals transmitted via the chip select lines (AAPA, Specification, [0023] and [0026]).

AAPA and Balasundram do not expressly teach the arrangement comprising wherein the arrangement comprising wherein the chip select signals transmitted via the chip select lines can be altered during the transmission of a frame.

Hastings further teaches an enabling signal (e.g. chip select signal) used by the slave (Fig. 3, ref. 304), wherein the enabling signal initiates the slave for transmission of data to the master and the enabling signal can be transmitted during the transmission of a frame, therefore can be altered from high to low or low to high during the transmission of the frame (Fig. 3, ref. 304).

It would have been obvious to one of ordinary skill in this art, at the time of invention was made to include Hastings's altering of the enable signal into AAPA and Balasundram's arrangement for the benefit of reducing the number of wires needed and increase data flow by reducing the flow of start and stop bits (Hastings, col. 1, ll. 29-55) to obtain the invention as specified in claim 22.

20. Claim 16 is rejected under 35 U.S.C. 103(a) as being unpatentable over AAPA in view of Balasundram et al. (US Pub.: 2003/0103519) and further in view of and "Data Communications Basics" as applied to claim 11 above, and further in view of Bishop (US Patent 6,154,509).

AAPA, Balasundram and "Data Communications Basics" teach all the limitations of claim 11 as discussed above, but AAPA, Balasundram and "Data Communications Basics" do not expressly teach the arrangement comprising wherein the first semiconductor chip ascertains the phase of the diagnostic data by oversampling the diagnostic data.

Bishop teaches a system and a method comprising a receiver oversampling an inputting signal, therefore able to proper determine the phase of the inputting signal (col. 1, ll. 36-40 and col. 1, ll. 50-55).

It would have been obvious to one of ordinary skill in this art, at the time of invention was made to include Bishop's oversampling of the inputting signal into AAPA, Balasundram and Data Communications Basics' apparatus for the benefit of providing noise immunity (Bishop, col. 1, l. 57) and reducing cost of the design (Bishop, col. 3, ll. 13-25) to obtain the invention as specified in claim 16. The resulting combination of the references further teaches the apparatus comprising wherein the first semiconductor chip oversampling the received diagnostic data in order to properly determine the correct phase of the received signal.

21. Claims 18-19 and 20 are rejected under 35 U.S.C. 103(a) as being unpatentable over AAPA in view of Balasundram et al. (US Pub.: 2003/0103519) as applied to claim 23 above, and further in view of Rehmann et al. (US Patent 6,578,940).

22. As per claims 18-19, AAPA and Balasundram teach all the limitations of claim 23 as discussed above, where AAPA further teaches the arrangement comprising wherein the second line is part of a second transmission channel which further comprises:

a transmission clock line (AAPA, Drawings, CLK1, CLK2 of Fig. 1) via which the first semiconductor chip transmits a transmission clock signal to the second semiconductor chip (AAPA, Specification, [0021]-[0022] and [0024]-[0025]);

a chip select line (AAPA, Drawings, CS1, CS2 of Fig. 1) via which the first semiconductor chip transmits a chip select signal to the second semiconductor chip, the chip select signal signaling to the second semiconductor chip the start and end of the transmission of data intended for the second semiconductor chip via the second data line (AAPA, Specification, [0023] and [0026]); and

the first semiconductor chip outputting output the load control data (i.e. DATA2), the pilot data (i.e. DATA1a) and the transmission clock signal (i.e. CLK1, CLK2) (AAPA, Specification, [0020]-[0026]).

AAPA and Balasundram do not teach the arrangement comprising:

a second transmission clock line …;

a third data line …; and

wherein output drivers on the first semiconductor chip are LVDS drivers … .

Rehmann teaches a system and a method comprising:

an electronic controller (Fig. 3, ref. 26) including a low-voltage differential signaling (LVDS) driver (Fig. 3, ref. 56), wherein the LVDS driver produces no spike currents (col. 2, ll. 7-8); and

transferring of data from the electronic controller's LVDS driver (Fig. 3, ref. 52) to a receiver (Fig. 3, ref. 56), wherein the LVDS driver has a non-inverted terminal (Fig. 4, ref. 78) and an inverted terminal (Fig. 4, ref. 80) (Fig. 3 and col. 5, ll. 25-28).

It would have been obvious to one of ordinary skill in this art, at the time of invention was made to include Rehmann's LVDS driver into AAPA and Balasundram's arrangement for the benefit of transferring data at very high rate, up to 1.5 gigabits per seconds and not producing any spike currents (Rehmann, col. 2, ll. 7-9) to obtain the invention as specified in claims 18-19. The resulting combination of the references further teaches arrangement comprising:

the first semiconductor including the LVDS driver, wherein the LVDS would limits electromagnetic interference as the LVDS driver produces no spike current; and

the LVDS' inverted terminal including the second transmission clock line for transferring the complementary transmission clock signal and the third data line for transmits the complementary load control data and complementary pilot data.

23. As per claim 20, AAPA and Balasundram teach all the limitations of claim 23 as discussed above, where both further teach the arrangement comprising wherein the second line is part of a second transmission channel which further comprises:

wherein the first semiconductor chip (e.g. single center transmitter) is coupled to a plurality of receivers for outputting the load control data, the pilot data and a transmission clock signal (AAPA , Specification, [0020]-[0025] and Balasundram, [0007]), and wherein a user of the arrangement is able to set which of the plurality of

receivers needs to be used in each case (Balasundram, [0007]), wherein the single center transmitter (i.e. first semiconductor chip) generates the encoded data specifying which of the receiver would receives the data.

AAPA and Balasundram do not expressly reaches the arrangement comprising the first semiconductor chip has a plurality of respective different output drivers for outputting data.

Rehmann teaches a system and a method comprising:

an electronic controller (Fig. 3, ref. 26) including a low-voltage differential signaling (LVDS) driver (Fig. 3, ref. 56), wherein the LVDS driver produces no spike currents (col. 2, ll. 7-8); and

transferring of data from the electronic controller's LVDS driver (Fig. 3, ref. 52) to a receiver (Fig. 3, ref. 56), wherein the LVDS driver has a non-inverted terminal (Fig. 4, ref. 78) and an inverted terminal (Fig. 4, ref. 80) (Fig. 3 and col. 5, ll. 25-28).

It would have been obvious to one of ordinary skill in this art, at the time of invention was made to include Rehmann's LVDS driver into AAPA and Balasundram's arrangement for the benefit of transferring data at very high rate, up to 1.5 gigabits per seconds and not producing any spike currents (Rehmann, col. 2, ll. 7-9) to obtain the invention as specified in claims 18-19. The resulting combination of the references further teaches arrangement comprising wherein the first semiconductor includes the LVDS driver for outputting the data to the respective second semiconductors.

(10) Response to Argument

I. claims 2-4, 6-8, 10, 12 and 23-25

Issue I

Appellant seems to argue (on page 7, 1st to 3rd paragraph) that Balasundram does not teach/suggest the claimed feature that a portion of data is intended for a first, second semiconductor chip, a portion of data in the same frame is intended for a second, second semiconductor chip, because Balasundram does not teach that a plurality of data is transferred utilizing a single allotted time interval (e.g. single frame), because data in a given multiple byte waveform message is received by only the receiver that recognizes the specific identifier address.

Examiner's response to Issue

The examiner respectfully disagrees, because Balasundram teaches time division multiplexing, wherein within a single frame allocated to include two identifier addresses, the first portion of data correspond to the first identifier address is then be intended for the first, second semiconductor chip, and the second portion of data correspond to the second identifier address is then be intended for the second, second semiconductor chip. Furthermore, Balasundram does teach a single transmitter transferring data to multiple receivers (Balasundram, [0006]-[0009] and [0046]).

Issue II

Appellant seems to argue (on page 7, 4th paragraph to page 8, 1st paragraph) that one of ordinary skilled in the art would not be motivated to combine the references to arrive at the result claimed feature that data is transmitted in frames using data on a chip select line, wherein the chip select line designates the load control data and pilot data frames for a specific address because Balasundram is nonanalogous art; as Balasundram teaches a time-division multiplexing system that requires header (i.e. identifier address, associated with data designated the destination for the data), whereas AAPA teaches the chip select line designates the beginning and the end of data transmission.

Therefore, because Balasundram requires a header to associate the data with the designate address, one skilled in the art would not look to Balasundram for any additional reaching with respect to the prior art.

Examiner's response to Issue

The examiner respectfully disagrees, because not only is Balasundram in the field of appellant's endeavor, wherein Balasundram is application is associated with transferring of control data associated with motor vehicle control units (Balasundram, Fig. 7 and Appellant's Specification, [0007]); furthermore, Balasundram's teaching is reasonably pertinent to the particular problem with which the appellant was concerned, which is to reduce the number lines utilized for communication between a control unit (e.g. system controller or microcontroller) and the corresponding device being controlled (e.g. actuated

devices) via time-division multiplexing (Balasundram, Fig. 7; [0006]; [0048] and Appellant's Specification, [00029]; [0031]; [0035]; [0052]).

Furthermore, the examiner clarifies as following as to how the references are relied upon for the teaching of the above claimed feature:

AAPA teaches that data is transmitted in using data on a chip select line, as CS1 data on the chip select line designates pilot data transmitted is for a first of a semiconductor chip (e.g. power chip) and a CS2 data on the chip select line designates load control data for a second of the semiconductor chip (Specification, [0022]-[0023] and [0025]-[0026]).

Balasundram teaches the transferring of data in frames from a single central transmitter to a plurality of receivers utilizing time-division multiplexing (Balasundram, [0006]-[0009] and [0046]).

Therefore, the resulting combination of the references further teaches data is transmitted in frames via time-division multiplexing designated by data on the chip select line.

(11) Related Proceeding(s) Appendix

No decision rendered by a court or the Board is identified by the examiner in the Related Appeals and Interferences section of this examiner's answer.

For the above reasons, it is believed that the rejections should be sustained.

Respectfully submitted,

Chun-Kuan Lee
Patent Examiner
Art Unit 2181

Conferees:

/Alford W. Kindred/
Supervisory Patent Examiner, Art Unit 2181

Kevin L. Ellis
/Kevin L Ellis/
Supervisory Patent Examiner, Art Unit 2117